## REMARKS

Claims 1-20 are pending. Claims 1, 8 and 21 have been amended herein. Claims 1, 8 and 21 as amended are fully supported in the detailed description. No new matter has been added to the specification.

## Section 35 U.S.C. 103 Rejection

Claims 1, 6, 8, 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Chisholm et al., Winkler et al. and Wilcox. Applicants respectfully submit that the embodiments that are set forth in Claims 1, 6, 8, 12 and 21 are not rendered obvious by Applicants' Admitted Prior Art (AAPA) in view of Chisholm et al., Winkler et al. and Wilcox.

In particular AAPA in view of Chisholm et al., Winkler et al. and Wilcox does not teach or suggest "a plurality of bypass registers coupled to the bus master controller, wherein each bypass register of the plurality of bypass registers has more than 8 bits is memory mapped and aggregates disk transaction information from memory mapped data transfers from a host CPU" as recited in Claim 1. (Claims 8 and 21 recite similar recitations).

AAPA discusses an ADMA specification that is designed to improve ATA type devices. As discussed, the ADMA specification is designed to add features that improve the data transfer speed and efficiency of ATA devices. Moreover, AAPA discusses several of the shortcomings of ADMA that are not addressed in the prior art. It should be appreciated that AAPA does not discuss a plurality of memory mapped registers such as

are recited in Claim 1 (Claims 8 and 21 recite similar recitations).

As understood by Applicants, Chisholm et al. purportedly discloses an information handling system for transfer of command blocks to a local processing side without local processor intervention (see abstract). In the outstanding Office Action host command address register set 311 is contended to teach the recited memory mapped bypass register (see outstanding Office Action, page 5). Applicants respectfully disagree. The command address register set 311 includes command channel host address register 410 and command channel control register 420. As discussed in Chisholm et al. command address register set 311 receives command block addresses for each of the host command blocks that are to be transferred from a host processing side to an address on a local processing side (see col. 5, lines 25-27 and 45-50). Moreover, in Chisholm et al. transfers of command blocks are based on addresses that the command address register set 311 receives that correspond to command blocks and not on the address register set 311 being memory mapped. It is apparent that the command address register sets 311 are not memory mapped because the addresses that it receives clearly change when it receives addresses corresponding to different command blocks. Accordingly, Chisholm et al. teaches away from a mapping of address register set 311 to memory and thus does not teach or suggest a memory mapped register as is recited in Claims 1, 8 and 21.

In addition, amended Claims 1, 8 and 21 recite that a "plurality of bypass registers" are coupled to the bus master controller. Assuming arguendo that the disclosed command address register sets 311 could be considered to be memory mapped, these limitations would not be met because Chisholm et al. teaches that only one register,

CHAR 410, of the disclosed address register set 311 is related to addresses (see col. 6, lines 12-20 where register CCCR 420 is associated with block count and register CHAR 410 is associated with command block memory addresses). Accordingly, Chisholm et al. cannot reasonably be considered to teach or suggest a plurality of bypass registers that are memory mapped as is recited in Claims 1, 8 and 21.

The relied upon Winkler et al. and Wilcox references do not remedy the deficiencies of AAA and Chisholm et al. discussed above as regards the aforementioned limitations related to the recited memory mapped registers. Accordingly, Applicants respectfully submit that AAA in view of Chisholm et al., Winkler et al. and Wilcox references do not teach or suggest the embodiment recited in Claims 1, 8 and 21.

## CONCLUSION

Applicants respectfully assert that all claims are now in condition for allowance and Applicants earnestly solicit such action from the Examiner. The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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Dated: November 30, 2010

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